



Patent Application *Rec.*
34650-00428

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
Alf Larsson et al.)
Serial No.: 09/306,684) Examiner: A. Luu
Filed: May 6, 1999) Group Art Unit: 2816

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OFFICE OF PETITIONS

For: SYSTEM AND METHOD FOR IMPLEMENTING A SKEW-TOLERANT TRUE-SINGLE-PHASE-CLOCKING FLIP-FLOP

BOX DAC
Assistant Commissioner for
Patents
Washington, D.C. 20231

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Signature	<i>Debbie Hargrove</i> DEBBIE HARGROVE

Dear Sir:

REQUEST FOR RECONSIDERATION

In response to the Office Action dated September 21, 2000, Applicant presents the following remarks:

The claims presently pending are Claims 1-14. Claims 7-14 have been allowed. Claims 3-6 have been indicated as being allowable if rewritten to include the base claim and any intervening claims. In the Detailed Action, the Examiner listed two rejections:

(1) Claims 1-6 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Specifically, the limitation of "an input for receiving first data and second data," on line 3 of Claim 1 was found to not be supported by the disclosure.

Applicant respectfully traverses the rejection of Claim 1. Sufficient disclosure to support that which is claimed can be found on page 14, line 19 - page 16, line 8 of the present application. The cited pages discuss two different data signals being received at the input "D" (shown in Fig. 5) at different times. At the rising edge of the first clock signal, the new input data signal (second data) is isolated, while at the rising edge of the second clock signal, previously stored data (first data) is driven towards the output. Therefore, Applicant respectfully submits that Claim 1 is not indefinite, and Claims 2-6 are likewise not indefinite for the reasons discussed above in connection with Claim 1.

(2) Claims 1-2 have been rejected under 35 U.S.C. 102(b) as being anticipated by Hanawa et al. (U.S. Pat. No. 4,745,302). On page 3 of the Detailed Action, the Examiner discusses the Hanawa et al. reference as showing a first flip-flop controlled by a first clock signal for receiving a first data, a combinational logic and

a second flip-flop controlled by a second clock signal and having an output for transmitting the data.

However, the Examiner did not mention or discuss the specifically claimed limitations in Claim 1 of:

(a) "said first and second clock signals having the same frequency and substantially the same phase;" or

(b) "wherein the arrival times of said first and second clock signals at said flip-flop are skewed."

As Applicant pointed out in the previous response filed on July 11, 2000, in Hanawa et al., the clock signals are shifted in phase. Therefore, Hanawa et al. teaches away from the limitation that the clock signals have substantially the same phase. In addition, as Applicant also pointed out in the previous response filed on July 11, 2000, there is no disclosure or suggestion in Hanawa et al. for the clock signals to be skewed in arrival time. As just mentioned, in Hanawa et al., the clock signals are shifted in phase, not in arrival time.

Therefore, Applicant respectfully submits that Claim 1 is patentable over the art of record. In addition, Applicant respectfully submits that Claim 2 is patentable over the art of record for the reasons recited above with respect to Claim 1.

Thus, all grounds of rejection and/or objection are traversed or accommodated, and favorable reconsideration and allowance are respectfully requested. The Examiner is respectfully requested to call the undersigned at the telephone number below if any further action by Applicant would facilitate the allowance of the application.

Respectfully submitted,

JENKENS & GILCHRIST, P.C.

Holly L. Rudnick

Holly L. Rudnick

Reg. No. 43,065

Dated: 5/15/01

1445 Ross Avenue, Suite 3200
Dallas, Texas 75202
(214) 855-4780
(214) 855-4300 (fax)

AL
Bill Bauer

214 - 855-4201